

Abstract

Electronic phase-locked loop (PLL)

The electronic phase-locked loop (PLL) of digital design is supplemented by an additional analog phase detector (APD), which enables the phase error ("jitter") to be attenuated in a manner even better than heretofore. The PLL is used in particular as an integrated circuit (IC) in integrated services communications networks (ISDN), data communication or networks.

Fig. 1

0989260.010302